

REMARKS

Claims 15-39 were previously pending, of which claim 15 has been cancelled without prejudice, claims 16-23 and 27 have been amended, and claims 24, 25, 28-29, and 31-39 have been maintained in their original form. Applicant respectfully submits that the present amendment places the claims either in condition for allowance or in better form for appeal. Additionally, the present amendment does not raise any new issues that would require further consideration and/or search. Reconsideration of presently pending claims 16-39 is respectfully requested in light of the following remarks.

Allowed Claims

Noted with appreciation is the indication in the Office Action that claims 26 and 30 have been allowed.

Allowable Subject Matter

Noted with appreciation is the indication in the Office Action that claims 17, 18, 20, 21, 25, 27, 29, 32, 33, and 37-39 are directed at allowable subject matter, and would be allowed if rewritten in independent form. These claims depend from rejected claims but, for reasons set discussed below, it is believed that the rejected claims are also allowable. Accordingly, it is believed to be unnecessary to rewrite claims 17, 18, 20, 21, 25, 27, 29, 32, 33, and 37-39 in independent form at this time.

Rejections Under 35 U.S.C. §102

Claim 28 recites:

A method of manufacturing a microelectronic device, comprising:
providing a substrate having a protective layer located thereon and a
plurality of isolation structures extending through the protective layer and at least

partially into the substrate, the substrate including at least one memory cell region
and at least one periphery region;

forming a mask over a at least a portion of the periphery region and
exposing at least a portion of the memory cell region;

removing sacrificial portions of the protective layer from within the
memory cell region;

removing the mask;

forming a conformal layer over remaining portions of the protective layer,
the isolation structures, and in voids created by the removal of the sacrificial
portions of the protective layer;

planarizing the conformal layer such that the conformal layer, the
isolation structures, and the remaining portions of the protective layer are
substantially coplanar;

removing the remaining portions of the protective layer; and

forming transistors in voids created by the removal of the remaining
portions of the protective layer.

Claim 28 was rejected under 35 U.S.C. §102(e) as being anticipated by Kim, et al. (US Patent No. 6,524,915 hereinafter referred to as “Kim”). The PTO provides in MPEP § 2131 that “[t]o anticipate a claim, the reference must teach every element of the claim....” Therefore, with respect to claim 28, to sustain this rejection the Kim patent must contain all of the above claimed elements of the claim. The Examiner alleges that “Kim shows the method as claimed in Fig. 7A-7O and corresponding text....” Applicant respectfully traverses this assertion. Applicant submits that the cited figures and corresponding text of Kim are directed at “a process of manufacturing a split-gate flash memory.” (See Kim, Col. 6, lines 36-39). Accordingly, Kim shows, in Fig. 6O & 7O, the completed split-gate flash memory. In contrast, claim 28 recites “providing a substrate having a protective layer located thereon and a plurality of isolation structures extending through the protective layer and at least partially into the substrate, the substrate including at least one memory cell region and at least one periphery region.” Thus, the

present application teaches a process directed to solving problems “attributable to topographic differences between memory devices and supporting [periphery] devices.” (See Present Application, par. [0005]).

For example, with regard to the claim 28 limitation of “forming a mask over a at least a portion of the periphery region and exposing at least a portion of the memory cell region,” the Examiner cites Col. 7, lines 9-20 of Kim as allegedly teaching this limitation. The cited passage reads as follows:

Referring to FIGS. 6B and 7B, a second oxidization film **205** is deposited over the entire surface of the semiconductor substrate **200** and covers the second nitride layer **204** and the exposed surface of the first conductive layer **202**. Even though not shown, before depositing the second oxidization film **205**, the first conductive layer **202** is etched using the second nitride layer **204** as a mask, or the exposed portion of the first conductive layer **202** is oxidized by an oxidation process, so that the exposed portion of the first conductive layer **202** is relatively thinner than the non-exposed portion thereof.

Nowhere in the cited passage of Kim does it teach, “forming a mask over a at least a portion of the periphery region and exposing at least a portion of the memory cell region,” as is recited in claim 28. Furthermore, the cited passage teaches that, “a second oxidization film [] is deposited over the entire surface of the semiconductor substrate.” Thus, Kim’s mask does not “expose[] at least a portion of the memory cell region,” as is recited in claim 28.

As another example, with regard to the claim 28 limitation of “planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar,” the Examiner cites Col. 7, lines 46-53 of Kim as allegedly teaching this limitation. The cited passage reads as follows:

Subsequently, as shown in FIGS. 6D and 7D, a second conductive layer is deposited over the whole surface of the semiconductor substrate **200** and is etched back to form the source line **209** that directly contacts the source junction region **207**. At this point, the source line **209** is insulated from the first conductive layer **202** by the oxidation spacer **206**.

Again, nowhere in the cited passage does it teach “planarizing the conformal layer such that the conformal layer, the isolation structures, and the remaining portions of the protective layer are substantially coplanar,” as is recited in claim 28. In fact, FIGS. 6D and 7D of Kim show features, such as isolation structures and conductive layers, that are not coplanar.

From the above, it is clear that rejection under 35 U.S.C. §102 with respect to claim 28 cannot be supported by the Kim reference and should be withdrawn.

Dependent Claims

Claims 16-23 and 27 have been amended to depend from, either directly or indirectly, and further limit allowed claim 26. Claims 24 and 25 depend from and further limit claim 23 which depends from and further limits allowed claim 26. Accordingly, claims 16-25 and 27 are in condition for allowance.


Claims 29 and 31-39 depend from, either directly or indirectly, and further limit independent claim 28 and, therefore are allowable for at least the same reasons as set forth above for claim 28.

Conclusion

It is clear from the foregoing that independent claims 26, 28, and 30 are in condition for allowance. Dependent claims 16-25, 27, 29, 31-39 depend from, either directly or indirectly, and further limit independent claims 26, 28, and 30, and therefore are allowable as well.

The Examiner is invited to call the undersigned at the below-listed telephone number if a telephone conference would expedite or aid the prosecution and examination of this application. Deposit account 08-1394 can be used, as required.


Respectfully submitted,



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I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on August 25, 2006
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